What is claimed is;

1. A method for manufacturing field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming an active nitride film formed on the SOI substrate;

patterning the active nitride for form a mask;

forming a field oxide film for element isolation with the mask;

wet-etching the mask until the film thickness thereof is reduce to allow an edge of the silicon layer contacting the field oxide film to be exposed;

implanting ions of a channel stopping impurity into the edge of the silicon layer by using the wet-etched mask; and

forming a gate electrode, a source and drain on the SOI substrate.

2. A method for manufacturing field effect transistor according to claim 1, wherein implanting ions of a channel stopping impurity vertically into the edge of the silicon layer.

3. A method for manufacturing field effect transistor according to claim 1, wherein implanting ions of a channel stopping impurity at an angle into the edge of the silicon layer.

4. A method for manufacturing field effect transistor according to claim 3, wherein the film thickness of the active nitride film is adjusted during the ion implantation in correspondence to the angle at which the ions are implanted.

5. A method for manufacturing field effect transistor according to claim 1, further comprising:

implementing a heat treatment on the SOI substrate after implanting ions of the channel stopping impurity.

6. A method for manufacturing field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of a nitride film before forming the field oxide film for element isolation.

7. A method for manufacturing field effect transistor according to claim 1, further comprising:

forming a silicon oxide film on an area where the edge of the silicon layer is exposed after wet-etching the mask.

8. A method for manufacturing field effect transistor according to claim 1, further comprising:

forming a silicon oxide film on an area where the edge of the silicon layer is exposed after implanting the ions of said channel stopping impurity.

9. A method for manufacturing field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of a silicon oxide film at a side surface of the active nitride film after implanting the ions of said channel stopping impurity.

10. A method for manufacturing field effect transistor according to claim 1, further comprising:

forming a sidewall constituted of a polysilicon film at a side surface of the active nitride film;

oxidizing the sidewall constituted of the polysilicon film after implanting the ions of said channel stopping impurity.

11. A method for manufacturing field effect transistor comprising:

providing an SOI substrate having a silicon layer formed on an insulating layer;

forming a gate electrode by etching a conductive layer formed on the silicon layer;

implanting ions to form a source and drain at an energy level at which all the impurity is injected into the silicon layer constituting the source and drain; and

implementing a heat treatment at a low temperature under 1000℃ in order to activate the impurity at the source and drain.

12. A method for manufacturing field effect transistor according to claim 11, further comprising:

forming an silicon oxide film or an silicon nitride film over a thickness of 10 ~ 30nm after forming the gate electrode.

13. A method for manufacturing field effect transistor according to claim 11, further comprising:

implanting ions of an N-type impurity over the surface of the silicon layer to achieve a concentration of $10^{18} \sim 10^{19}$ cm^{-3} ; and

forming an silicon oxide film or an silicon nitride film over a thickness of 10 ~ 30nm after forming the gate electrode.

14. A method for manufacturing field effect transistor according to claim 11, wherein:

the impurity in the gate electrode becomes activated before forming the gate electrode.

15. A method for manufacturing field effect transistor according to claim 11, further comprising:

forming an silicon oxide film or an silicon nitride film over a thickness of 10 ～ 30nm after forming the gate electrode; and

becoming activated the impurity in the gate electrode before forming the gate electrode.

16. A method for manufacturing field effect transistor according to claim 11, further comprising:

implanting ions of an N-type impurity over the surface of the silicon layer to achieve a concentration of $10^{18} \sim 10^{19}$ cm^{-3} ;

forming an silicon oxide film or an silicon nitride film over a thickness of 10 ～ 30nm after forming the gate electrode; and

becoming activated the impurity in the gate electrode before forming the gate electrode.

17. A method for manufacturing field effect transistor according to claim 11, wherein:

the impurity concentration at the source and drain is set at 10^{20} cm^3 or higher and at a lowest possible concentration level which does not increase the contact resistance of Co silicide and Si.

18. A field effect transistor manufacturing method according to claim 11, wherein:

the ions implanted at said source and drain is implemented twice, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration; and

the heat treatment is performed to activate said impurity at said source and drain at a low temperature below 950°C is implemented.

19. A field effect transistor manufacturing method according to claim 11, wherein:

the ions implanted at said source and drain is implemented twice, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration;

the impurity concentration near the surface of said silicon layer is set equal to or higher than $10^{20}cm^{-3}$ through the ion implantation implemented at the low energy level achieving the high concentration with the impurity concentration becoming lower toward the rear surface of said silicon layer; and

the heat treatment is performed to activate said impurity at said source and drain at a low temperature below 950°C is implemented.

20. A field effect transistor manufacturing method according to claim 11, wherein:

the ions implanted at said source and drain is implemented twice, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration;

the impurity concentration near the rear surface of said silicon layer is set higher than the channel concentration and equal to or lower than $10^{19}cm^{-3}$ through the ion implantation implemented at the high energy level achieving the low concentration; and

the heat treatment is performed to activate said impurity at said a source and drain at a low temperature of last on 950°C is implemented.

21. A field effect transistor manufacturing method according to claim 11, wherein:

the ions implanted at said source and drain is implemented twice, once at a low energy level achieving a high concentration and another time at a high energy level achieving a low concentration;

the impurity concentration near the rear surface of said silicon layer is set higher than the channel concentration and equal to or lower than $10^{19}cm^{-3}$ through the ion implantation implemented at the high energy level achieving the low concentration;

the impurity concentration near the surface of said silicon layer is sets equal to or higher than $10^{20}cm^{-3}$ through the ion implantation implemented at the low energy level achieving the high concentration with the impurity concentration becoming lower toward the rear surface of said silicon layer; and

the heat treatment is performed to activate said impurity at said source and drain at a low temperature below 950°C is implemented.